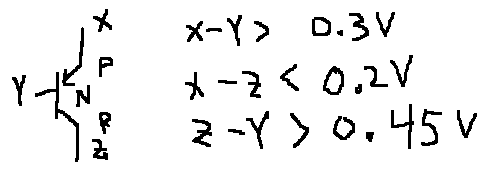
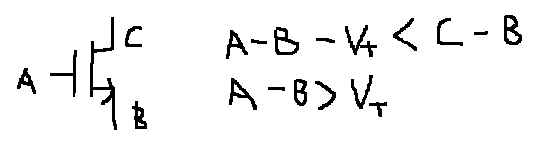
1a) 

1b) 

2a) None. No power is used on H to L transitions. C discharges but no energy taken from supply.

2b) 

2c)



3a) Q2 CBC, Q3 CBC

3b) 2 CBC

3c) CBE2+2CBC2

4a) Static (leakage), dynamic, short-circuit

4b) Static: Off but leaks, Dynamic: Switching, Short-circuit: When both are on during transition

4c) Dynamic store value on C, Static provide voltage by providing low impedance path to supply or GND

4d) Where the size of the devices decide output voltage (ratioed)

4e) ROM: Read only, RAM: Read/write

4f) RAM/ROM: Random access, Stack: can’t randomly access memory

4g) DRAM smaller

4h) Slower

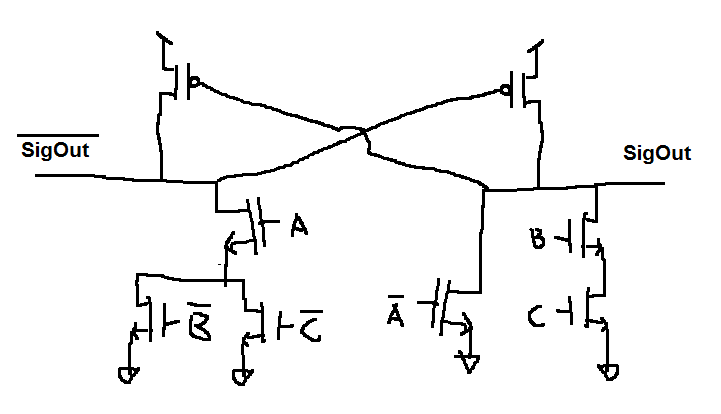
4i) Lower VDD used inside memory. Need to restore V to circuit V.

4j)tr: 10% to 90% single wire. Tf: 90% to 10% single wire. tpHL: 50% input to 50% output, tpLH same

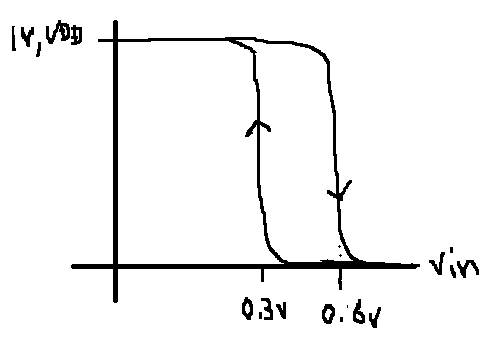
4k) BL(3:0)=1010 BL(0:3)=0101

5) DCVSL: SigOut=





6)



7a) Max(

tclkQ0+td+tsu1=9ns+5ns+20ns=34ns

tclkQ1+td+tsu2=11ns+5ns+20ns=36ns

tclkQ1+tsu0=11ns+10ns=21ns ) = 36ns or f=1/36ns

7b) tclkQ0+td < th1? 🡺 5ns+3ns=8ns < 6ns? No

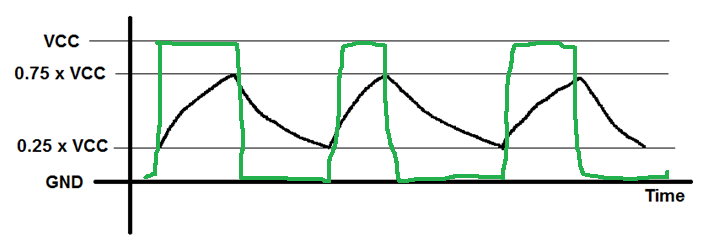
tclkQ1+td < th1? 🡺 2ns+3ns=5ns < 6ns? Yes

tclkQ1 < th0? 🡺 2ns < 6ns? Yes

2 violations.

8a) Rcenter=2Rtop=2Rbottom

8b)



9a) CMOS, , Vout**MAX**=VDD, Vout**MIN**=GND.

9b) (P)ECL, ,, Vout**MAX**=VDD-VBEON,

Vout**MIN**=.

10a) b) Vout min gets lower

